AMENDMENTS TO THE CLAIMS

1-26. (Canceled).

27. (Previously presented) An array of resistance variable memory cells comprising:

at least one pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode, a chalcogenide glass layer having metal ions diffused therein in contact with the first electrode and being capable of changing resistance under the influence of an applied voltage, a metal layer in contact with the chalcogenide glass layer, and a second electrode in contact with the metal layer, the at least one pillar not located within a via.

28-48. (Canceled).

49. (Currently amended) The array of [[Claim]] claim 27, wherein the metal ions comprise silver ions.

50. (Currently amended) The array of [[Claim]] claim 27, wherein at least one of the first and second electrodes is tungsten.

51. (Currently amended) The array of [[Claim]] claim 27, wherein the metal layer comprises silver.

52. (New) The array of claim 27, wherein the chalcogenide glass layer comprises silver germanium sulfide.

53. (New) A memory array comprising:

at least one pair of memory cells, the cells comprising pillars of stacked material layers on a semiconductor substrate, the stacked layers comprising a shared first electrode, separate chalcogenide glass layers having metal ions diffused therein in contact with the shared first electrode and being capable of changing resistance under the influence of an applied voltage, separate metal layers in contact with each of the chalcogenide glass layers, and separate second electrodes in contact with each of the metal layers, the pillars not being located within vias.

53. (New) The array of claim 53, wherein the metal ions comprise silver ions.

54. (New) The array of claim 53, wherein the shared first electrode is tungsten.

55. (New) The array of claim 53, wherein at least one of the second electrodes is tungsten.

56. (New) The array of claim 53, wherein at least one of the metal layers comprise silver.

57. (New) The array of claim 53, wherein the chalcogenide glass layer having metal ions diffused therein comprises silver germanium sulfide.

58. (New) A processor system, comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising a memory array, the memory array comprising:

a plurality of memory units comprising stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode, a chalcogenide glass layer having metal ions diffused therein in contact with the first electrode and being capable of changing resistance under the influence of an applied voltage, a metal layer in contact with the chalcogenide glass layer, and a second electrode in contact with the metal layer, the at least one pillar not located within a via.

59. (New) The processor system of claim 58, wherein the metal ions comprise silver ions.

60. (New) The processor system of claim 58, wherein at least one of the first and second electrodes is tungsten.

61. (New) The processor system of claim 58, wherein at least one of the metal layers comprise silver.

62. (New) The processor system of claim 58, wherein the chalcogenide glass layer having metal ions diffused therein comprises silver germanium sulfide.